

1 **CLAIMS**

2 **1.** A method of processing data using a transmit parallel interface
3 comprising:

4 providing a system clock signal associated with data in a first clock
5 domain;

6 providing a high speed clock signal relative to the system clock signal;

7 dividing the high speed clock signal to provide a clock signal in a second
8 clock domain; and

9 clocking data using the clock signal in the second clock domain.

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11 **2.** The method of claim 1, wherein said providing the high speed clock
12 signal comprises providing a high speed clock signal that is N times faster than the
13 system clock signal.

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15 **3.** The method of claim 1, wherein said providing the high speed clock
16 signal comprises providing a high speed clock signal that is N times faster than the
17 system clock signal, where N is greater than or equal to 4.

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19 **4.** The method of claim 1, wherein:
20 said providing the system clock signal comprises providing the system
21 clock signal at a first frequency; and
22 said dividing the high speed clock signal comprises dividing the high speed
23 clock signal such that the clock signal in the second clock domain is provided at
24 the first frequency.
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1 5. The method of claim 1, wherein the system clock signal has rising
2 and falling clock edges, and said dividing the high speed clock signal to provide
3 the clock signal in the second clock domain comprises doing so in a manner that
4 places a rising edge of the clock signal in the second clock domain around the
5 falling edge of the system clock signal.

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7 6. A method of processing data using a transmit parallel interface
8 comprising:

9 clocking input data, in a parallel state, using a first clock signal to produce
10 clocked input data, the first clock signal having a frequency;

11 clocking a reset signal using the system clock signal to produce a clocked
12 reset signal;

13 clocking the clocked reset signal using a high speed clock signal to produce
14 an output signal;

15 receiving both the high speed clock signal and the output signal with a
16 divider circuit;

17 using the output signal to reset the divider circuit effective to produce a
18 second clock signal having a frequency that is the same as the frequency of the
19 first clock signal; and

20 re-clocking the clocked input data using the second clock signal.

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22 7. The method of claim 6, wherein said using of the output signal to
23 reset the divider circuit produces a second clock signal having a rising edge close
24 to a falling edge of the first clock signal.

1 8. The method of claim 6 further comprising after said re-clocking,
2 serializing re-clocked input data for transmission in a serial state.

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4 9. The method of claim 6, wherein the clocked reset signal and the
5 clocked input data are matched.

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7 10. The method of claim 6, wherein the first clock signal is of a
8 dividable frequency of the high speed clock signal.

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10 11. A transmit parallel interface comprising:
11 a single chip;
12 integrated circuitry on the chip configured to:
13 clock input data, in a parallel state, using a first clock signal to
14 produce clocked input data, the first clock signal having a frequency;
15 clock a reset signal using the system clock signal to produce a
16 clocked reset signal;
17 clock the clocked reset signal using a high speed clock signal to
18 produce an output signal;
19 receive both the high speed clock signal and the output signal with a
20 divider circuit;
21 produce, with the divider circuit, a second clock signal that has a
22 frequency that is the same as the frequency of the first clock signal; and
23 re-clock the clocked input data using the second clock signal.
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1 **12.** A transmit parallel interface comprising:
2 a first circuit to receive a clocked reset signal and a high speed clock signal
3 and produce therefrom an output signal, the clocked reset signal being clocked by
4 a system clock signal associated with a first clock domain and having a first
5 frequency; and
6 a second circuit to receive the high speed clock signal and the output signal
7 from the first circuit to produce therefrom a clock signal in a second clock domain,
8 said second clock domain clock signal having a second frequency that is the same
9 as the first frequency of the system clock signal.

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11 **13.** The transmit parallel interface of claim 12, wherein the second
12 circuit comprises a divider circuit.

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14 **14.** The transmit parallel interface of claim 12, wherein the second
15 circuit produces its clock signal such that a rising edge of the produced clock
16 signal is located close to a falling edge of the system clock signal.

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18 **15.** The transmit parallel interface of claim 12, wherein the system clock
19 signal is at a dividable frequency of the high speed clock signal.

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21 **16.** The transmit parallel interface of claim 12, wherein the high speed
22 clock signal is greater than or equal to 4 times faster than the system clock signal.

1 **17.** The transmit parallel interface of claim 12, wherein the first circuit
2 comprises one or more flip flops that are clocked by the high speed clock signal.

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4 **18.** The transmit parallel interface of claim 12, wherein the first and
5 second circuits are disposed on a single chip.

6
7 **19.** A transmit parallel interface comprising:
8 a first assembly of one or more flip flops configured to receive input data in
9 a parallel state and clock the input data using a system clock signal to produce
10 clocked input data, the system clock having a frequency;

11 a second assembly of one or more flip flops configured to receive a reset
12 signal and clock the reset signal with the system clock signal to produce a clocked
13 reset signal;

14 a third assembly of one or more flip flops configured to receive the clocked
15 reset signal and clock the clocked reset signal with a high speed clock signal to
16 produce an output signal;

17 a circuit configured to receive the output signal and the high speed clock
18 signal and produce therefrom a clock signal that has the same frequency as the
19 system clock signal;

20 a fourth assembly of one or more flip flops configured to receive the
21 clocked input data and re-clock the clocked input data using the clock signal
22 having the same frequency as the system clock; and

23 a serializer to serialize the re-clocked clocked input data.
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1 **20.** The transmit parallel interface of claim 19, wherein the system clock
2 signal is a dividable frequency of the high speed clock signal.

3
4 **21.** The transmit parallel interface of claim 19, wherein the first, second,
5 third and fourth assemblies of flip flops, as well as said circuit and serializer are
6 disposed on a single integrated circuit chip.

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8 **22.** The transmit parallel interface of claim 19, wherein said circuit
9 comprises a divider circuit.

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11 **23.** The transmit parallel interface of claim 19, wherein said circuit
12 comprises a $1/N$ divider circuit, where N is greater than or equal to 4.

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14 **24.** The transmit parallel interface of claim 19, wherein said clock signal
15 having the same frequency as the system clock is produced to have a rising edge
16 located very close a falling edge of the system clock signal.